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10/586,658	08/06/2008	Takuji Maeda	0074/075001	7735

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EXAMINER
AYASH, MARWAN

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/586,658	MAEDA ET AL.
	Examiner	Art Unit	
	MARWAN AYASH	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2006*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

  4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  a)☒ All   b)☐ Some *   c)☐ None of:

  1.☒ Certified copies of the priority documents have been received.

  2.☐ Certified copies of the priority documents have been received in Application No. _____.

  3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date <u>7/19/06, 2/7/07</u>.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____ .

DETAILED ACTION

Specification

1.   The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed. The following title is suggested:

Semiconductor memory device including device information storage containing erase block size

of a non-volatile memory.

Claim Objections

2.   **Claim 4 is objected to** because "…controller performs only <u>format processing of</u>

<u>constructing file system</u> so that an access…" appears grammatically and/or idiomatically

incorrect. Appropriate correction is required.

3.   **Claim 7, 13 are objected to** because the limitations "…determines an access unit to

optimally access to said nonvolatile memory …" and "…as a length of multiples of the optimum

access unit…" appear grammatically and/or idiomatically incorrect. Appropriate correction is

required.

4.   **Claims 8-9, 14-15 are objected to** because "…access unit to optimally access to said

nonvolatile memory …" appears grammatically and/or idiomatically incorrect. Appropriate

correction is required.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United
> States before the invention thereof by the applicant for patent, or on an international application by another who
> has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention
> thereof by the applicant for patent.
> The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the
> Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference
> is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.
> Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the

AIPA (pre-AIPA 35 U.S.C. 102(e)).

6.   **Claims 1-15 are rejected** under 35 U.S.C. 102(e) as being anticipated by Sasaki et al.
(US PGPub # 20050036372)

With respect to **independent claims 1, 11** Sasaki discloses a semiconductor memory
device & control method comprising:

a nonvolatile memory that consists of a plurality of sectors [*Sasaki abstract, 0068*], a
certain number of continuous sectors of which are grouped as a block of a minimum unit for data
erase [*Sasaki abstract, 0068*], and writes or reads data transmitted from an external access device
[*Sasaki abstract*];

a memory controller for controlling erase, writing and reading of data to said nonvolatile
memory when a command containing a control signal is input from said access device [*Sasaki
abstract*];

a device information storage part for storing device information concerning physical
properties of the semiconductor memory device containing erase block size of said nonvolatile
memory [*Sasaki abstract, 0010, 0066, 0083, 0124*]; and

a file system interface controller for performing file access processing to said nonvolatile
memory on the basis of the device information stored in said device information storage part
[*Sasaki 0004-0005. 0010, 0044, 0055*].

With respect to **dependent claims 2, 12** as applied to claims 1, 11 Sasaki discloses
wherein said file system interface controller manages data stored in said nonvolatile memory as a
file and when a command to request file access processing to a file on said nonvolatile memory
is input from said access device, performs file access processing to a file existing in said
nonvolatile memory [*Sasaki 0055-0056*].

With respect to **dependent claim 3** as applied to claim 1 Sasaki discloses wherein said
nonvolatile memory has a first area and a second area [*Sasaki 0065*], said file system interface
controller manages data stored in said first area as a file and when a command to request file
access processing to a file in said first area of said nonvolatile memory is input from said access
device, performs file access processing to a file existing in said first area of said nonvolatile
memory, said semiconductor memory device further comprises: a low-level IO interface
controller for performing writing or reading processing of the data to said second area of said

nonvolatile memory, when a command to request writing or reading processing of the data to said second area of said nonvolatile memory is input from said access device for controlling file systems [*Sasaki 0065, 0068-0069*].

With respect to **dependent claim 4** as applied to claim 1 Sasaki discloses a low-level IO interface controller for performing writing or reading processing of data to an arbitrary position in said nonvolatile memory [*Sasaki 0044-0045*], when a command to request writing or reading processing of data to an arbitrary position of said nonvolatile memory is input from said access device for controlling file systems, wherein said nonvolatile memory has a common area controlled by both of said file system interface controller and said low-level IO interface controller [*at least control elements 31 and 37 have access to common storage in memory 38 (Sasaki Fig. 5)*]; said file system interface controller performs only format processing of constructing file system so that an access unit may be an optimum access unit on the basis of device information stored in said device information storage part to the common area on said nonvolatile memory [*Sasaki 0083, 0086-0088*]; and file access processing other than the format processing to a file existing in the common area on said nonvolatile memory is executed by said low-level IO interface controller on the basis of the command input from said access device [*Sasaki claim 1*].

With respect to **dependent claim 5** as applied to claim 1 Sasaki discloses wherein when a command to request read-only file access processing to a file on said nonvolatile memory is input from said access device, said file system interface controller performs file access processing to a file existing in said nonvolatile memory [*Sasaki 0077, 0140*], said semiconductor memory device further comprises: a low-level IO interface controller for performing writing or reading processing of data at the arbitrary position in said nonvolatile memory, when a command to request writing or reading processing of data at an arbitrary position in the area in said nonvolatile memory that said file system interface controller for data reading is input from said access device that controls the file system [*Sasaki 0044-0045*]; and a synchronization controller for updating file system management information read in a temporary storage memory in said semiconductor memory device by said file system interface controller so as not to cause inconsistency [*Sasaki 0005, 0048*], when said low-level IO interface controller performs data

writing processing to management information of the file system existing in said nonvolatile memory [*Sasaki 0005, 0048*].

With respect to **dependent claim 6** as applied to claim 1 Sasaki discloses wherein said device information storage part stores information on physical properties of the semiconductor memory device including erase block size of said nonvolatile memory and device information including a file system type flag representing a type of the file system built on the nonvolatile memory [*Sasaki 0066, 0072, 0077-0079, 0083*], said file system interface controller consists of a plurality of file system interface controllers for managing data stored in said nonvolatile memory on the basis of device information stored in said device information storage part and for performing file access processing to a file on the nonvolatile memory according to a command input from said access device [*Sasaki 0066, 0072, 0077-0079, 0083*], and said file system interface controller corresponding to said file system type flag among said plurality of file system interface controllers operates on said semiconductor memory device [*Sasaki 0085*].

With respect to **dependent claims 7, 13** as applied to claims 1, 11 Sasaki discloses wherein said file system interface controller determines an access unit to optimally access to said nonvolatile memory on the basis of information containing erase block size stored in said device information storage part [*Sasaki 0085-0088*], and sets the size of a management information area of a file system as a length of multiples of the optimum access unit when performing format processing of building the file system in an area of said nonvolatile memory [*Sasaki 0085-0088*].

With respect to **dependent claims 8, 14** as applied to claims 1, 11 Sasaki discloses wherein said file system interface controller determines an optimum access unit to optimally access to said nonvolatile memory on the basis of information containing erase block side stored in said device information storage part, and uses said optimum access unit as an area allocation unit when recording file data to said semiconductor memory device [*Sasaki 0085-0088*].

With respect to **dependent claims 9, 15** as applied to claims 1, 11 Sasaki discloses wherein said file system interface controller determines the optimum access unit to optimally access to said nonvolatile memory on the basis of information containing erase block size stored in said device information storage part, and allocates directory areas so that a plurality of directory areas are included in the same said optimum access unit [*Sasaki 0085-0088*].

With respect to **dependent claim 10** as applied to claim 1 Sasaki discloses wherein said file system interface controller is composed of a program stored in a memory as a nonvolatile updatable recording medium, and said file system interface controller can be replaced, updated or deleted from the outside of said semiconductor memory device [*software and hardware facilitate file system activity and any software stored may be updated, replaced and/or deleted using format or write commands*].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. When responding to this Office Action, <u>**any new claims and/or limitations should be accompanied by a reference as to where the new claims and/or limitations are supported in the original disclosure**</u>.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marwan Ayash at 571-270-1179. The examiner can normally be reached on Mon-Fri 10am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The examiner may be reached via email for unofficial correspondence at marwan.ayash@uspto.gov. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Marwan Ayash -- Examiner -- Art Unit 2185

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185